Amendments to the Specification

Please replace para. [0020] with the following:

FIG. 4B shows a storage scheme for the parity data according to the present invention. A data parity block 450 includes a parity data portion 460 and appended information 470. Appended information 470 includes a "Reference Tag" ("REF TAG"), usually a "Parity Virtual Block Address" ("Parity VBA)", portion 472, a "Metadata Tag" ("META TAG"), usually a "Logical Unit ID" with other possible "metadata" flags, portion 474 and a check sum ("CHECK SUM") portion 476. Reference Tag portion 472 when qualified by a "Parity" flag in Metadata Tag portion 474 contains information that identifies the so-called "sliver" for which parity data portion 460 provides redundancy. In particular, the "Parity Virtual Block Address" in the DIF of the parity block may specify the "Virtual Block Address" ("VBA") of the data block with the lowest such address of the RAID "sliver" (where address in this context means address in the virtual unit). Check sum portion 476 contains information that is used to detect errors in parity data portion ~~410~~ 460. Metadata Tag portion 474 contains additional portions 474A and 474B. Portion 474B can contain information about the device, such as a device identifier ("Logical Unit ID"). Portion 474A, according to the present invention, can contain a bit that is a function of the other DRQ-bits in portions 424A. The DRQ parity bit can be generated by an exclusive-OR function of all the other data block DRQ-bits. To illustrate, the 1-bit portions 424A can be exclusive-ORed together to generate the single DRQ parity bit that will saved in portion 474A. Generally, then, the DRQ parity bit is created as a function of the other DRQ bits in portions 424A in the same sliver.